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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/761,253	01/16/2001	Zhenhua Wang	PHCH 000002	5183

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/761,253	WANG, ZHENHUA	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11-19 and 21-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19,22 and 25* is/are allowed.

6)☒ Claim(s) *1,3-5,7,11,12,15,18,21,23 and 24* is/are rejected.

7)☒ Claim(s) *2,6,8,9,13,14,16 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed 06/21/04. The allowable subject matter of claims 10-14 has been withdrawn.

Claim objection

Claim 12 is objected to recite the secondary current source including the second transistor 44. However, the specification teaches that transistor 44 is part of the sensitive resistor 49.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3-5, 7, 11, 12, 15, 18, 21, 23 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Ito et al. (USP 5744998).

As to claims 1 and 18, Ito discloses in figure 8 a voltage level monitoring circuit, comprising: a first reference current source (15a) for generating a first reference current; a second reference current source (20a) for generating a second reference current; a controllable switch (17a); a monitoring current source (13a) for generating a monitoring current derived from a voltage (VPP) to be measured, the monitoring current source including: a primary current source (19a) for generating a primary current (current that going through 19a); a secondary current source (14a) for generating the monitoring current; and a process sensitive resistor (5a or 13a) connected in series with the primary current source *(The American Heritage Dictionary of the English Language, third Edition, defines that resistor is "a device used to control current in*

an electric circuit by providing resistance); and a comparator device (16a) including a first current input (+) coupled for receiving the first reference current in response to the controllable switch being non-conductive, and for receiving both the first reference current and second reference current in response to the controllable switch being conductive, a second current input (-) coupled for receiving the monitoring current, and at least one measuring signal output (/EN), wherein the comparator device is arranged for comparing the currents received at its two current inputs and for generating at the measuring signal output a measuring signal (/EN) with a first value (low) when the current received at its second current input is less than the current received at its first current input, and with a second value (high) when the current received at its second current input is more than the current received at its first current input.

As to claim 3, figure 8 shows a current output of the second reference current source (20a) is coupled to the comparator device (16a) through the controllable switch (17a).

As to claim 4, figure 8 shows the controllable switch (17a) is controlled by a control signal (EN) generated by the comparator device.

As to claims 5 and 21, figure 8 shows the control signal (EN) renders the controllable switch conductive when the a magnitude of the current received at the first input of the comparator device is higher than a magnitude of the current received at the second input of the comparator device, and renders the controllable switch non-conductive when the magnitude of the current received at the first input of the comparator device is lower than the magnitude of the current received at the second input of the comparator device.

As to claim 7, figure 8 shows the controllable switch (17a) includes a PMOS transistor having its source coupled the current output of the second reference current source, having its

drain coupled to the first current input of the comparator device, and having its gate coupled to a control output of the comparator device.

As to claim 11, figure 8 shows that the primary current source (19a) includes a PMOS transistor having its source connected to the voltage (Vpp) to be monitored, having its gate coupled for receiving a bias voltage (Vref4), and having its drain connected to a first terminal of the process sensitive resistor (13a).

As to claim 12, figure 8 shows that the secondary current source includes: a first NMOS transistor (14a) having its source connected to ground and its drain coupled to the second current input of the comparator device; and a second NMOS transistor (13a) having its source connected to ground and its drain connected to a resistive block (5a) of the process sensitive resistor (5a), wherein gates of the first and second NMOS transistors are connected together and to the drain of the second NMOS transistor.

As to claim 15, figure 8 shows the monitoring current source includes a programmable current source (the current that going through transistor 14a is varied in responsive to Vcmp. Thus, transistor 14a is a programmable current source).

As to claims 23 and 24, figure 8 shows the second reference current source and the switch are electrically connected in series in response to the switch being conductive; and the first reference current source is electrically connected in parallel to the series connection of the second reference current source and the switch in response to the switch being conductive.

Allowable Subject Matter

3. Claims 2, 6, 8, 9, 13, 14, 16, 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 19, 22 and 25 are allowed.

Claim 2 would be allowable because the prior art fails to teach or suggest the first reference current source (5) includes a PMOS transistor (50) having its source coupled for receiving the voltage to be measured, having its gate coupled for receiving a bias voltage, and having its drain coupled to the first current input (1 1) of the comparator device.

Claim 6 would be allowable because the prior art fails to teach or suggest the second reference current source includes a PMOS transistor having its source coupled for receiving the voltage to be measured, having its gate coupled for receiving a bias voltage (Vbias), and having its drain coupled to the controllable switch.

Claims 8-9 would be and claims 19, 11 and 25 are allowable because the prior art fails to teach the comparator circuit comprising first and second inverters connected in series between the input and output of the comparator device.

Claims 13 and 14 would be allowable because the prior art fails to teach or suggest that the process sensitive resistor includes a further PMOS transistor having its gate terminal connected to its drain terminal in a gate/drain node and having its source terminal coupled to the current output of the primary current source for receiving the primary current.

Claims 16 and 17 would be allowable because the prior art fails to teach or suggest the first and second reference current source including a programmable current source.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quan Tra
Patent Examiner

August 5, 2004